SB-3625XKX SYNCHRO/RESOLVER-TO-DIGITAL PCIE INTERFACE BOARD HARDWARE MANUAL

MN-3625XKX-001

105 Wilbur Place
Bohemia, New York 11716-2426
Tel: (631) 567-5600, Fax: (631) 567-7358
World Wide Web - http://www.ddc-web.com

For Technical Support - 1-800-DDC-5757 ext. 7771
United Kingdom - Tel: +44-(0)1635-811140, Fax: +44-(0)1635-32264
France - Tel: +33-(0)1-41-16-3424, Fax: +33-(0)1-41-16-3425
Germany Tel: +49-(0)89-15 00 12-11, Fax: +49-(0)89-15 00 12-22
Japan - Tel: +81-(0)3-3814-7688, Fax: +81-(0)3-3814-7689
Asia - Tel: +65 6489 4801
India - Tel: +09-080-301-200

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A	5/2016	All	Initial Release
B	12/2017	14, 15	Added section 6.2.4, and figures 6 and 7.
C	2/2018	5	Accuracy section of Spec table updated.
D	2/2019	8, 9, 11	Updated connector pinout table to match mating connector figure. Aligned channel enumeration pinout to match software.

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2 PREFACE

This manual uses typographical conventions to assist the reader in understanding the content. This section will define the text formatting used in the rest of the manual

2.1 Text Usage

- **BOLD**–indicates important information and table, figure, and chapter references.
- `Courier New`–indicates code examples.
- <…> - indicates user-entered text or commands.

2.2 Special Handling and Cautions

The SB-3625XKX series uses state-of-the-art components, and proper care should be used to ensure that the device will not be damaged by Electrical Static Discharge (ESD), physical shock, or improper power surges and that precautions are taken to avoid electrocution.

Warnings: Turn off power to the computer hardware and unplug from wall.

NEVER insert or remove board with power turned on.

Ensure that standard ESD precautions are followed. As a minimum, one hand should be grounded to the power supply in order to equalize the static potential.

Do not store disks in environments exposed to excessive heat, magnetic fields or radiation.

2.3 Trademarks

All trademarks are the property of their respective owners.

2.4 What is included in this manual?

This manual contains a hardware guide for the SB-3625XKX PCIe Board and a basic overview of the software supplied with the board. The Synchro API Library and Driver installations for Windows will be covered in the separate SB-36040S0 manual, as well as LabVIEW™ Support Software for Windows.

2.5 Technical Support

In the event that problems arise beyond the scope of this manual, you can contact DDC by the following:

US Toll Free Technical Support:
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Outside of the US Technical Support:
1-631-567-5600, ext. 7771

Fax:
1-631-567-5758 to the attention of Motion Feedback Technologies Applications

DDC Website:
www.ddc-web.com/ContactUs/TechSupport.aspx

Please note that the latest revisions of Software and Documentation are available for download at DDC's Web Site, www.ddc-web.com.

3 OVERVIEW

The SB-3625XKX PCIe board provides intelligent interfacing between a Synchro or Resolver's output and a PCIe Bus.

3.1 Features

- Plug-and-Play (PnP) compatible for easy installation
- Utilizes RD-19230 converters
- Software-Programmable Resolution (10,12,14 or 16 bits)
- Software-Programmable Bandwidth
- Self-Test

MFBA GUI software has the capability to display position for either eight channels of single speed or four channels of two-speed. Also included with each board is the Synchrolib.dll Runtime Library with sample code that allows users to easily write their own software for the board. Please refer to the SB-36030S0 Software Manual available on our website *www.ddc-web.com* for installation and function call information.

To install the latest official software from DDC, download via DDC's website at *www.ddc-web.com/Products/CardsMatrixSynchroResolver.aspx*. Navigate to the applicable product page and click on the software tab. A download link will be given for the latest package(s) at no cost. System Requirements

3.2 System Requirements

The PC must be configured with a Windows or Linux operating system.

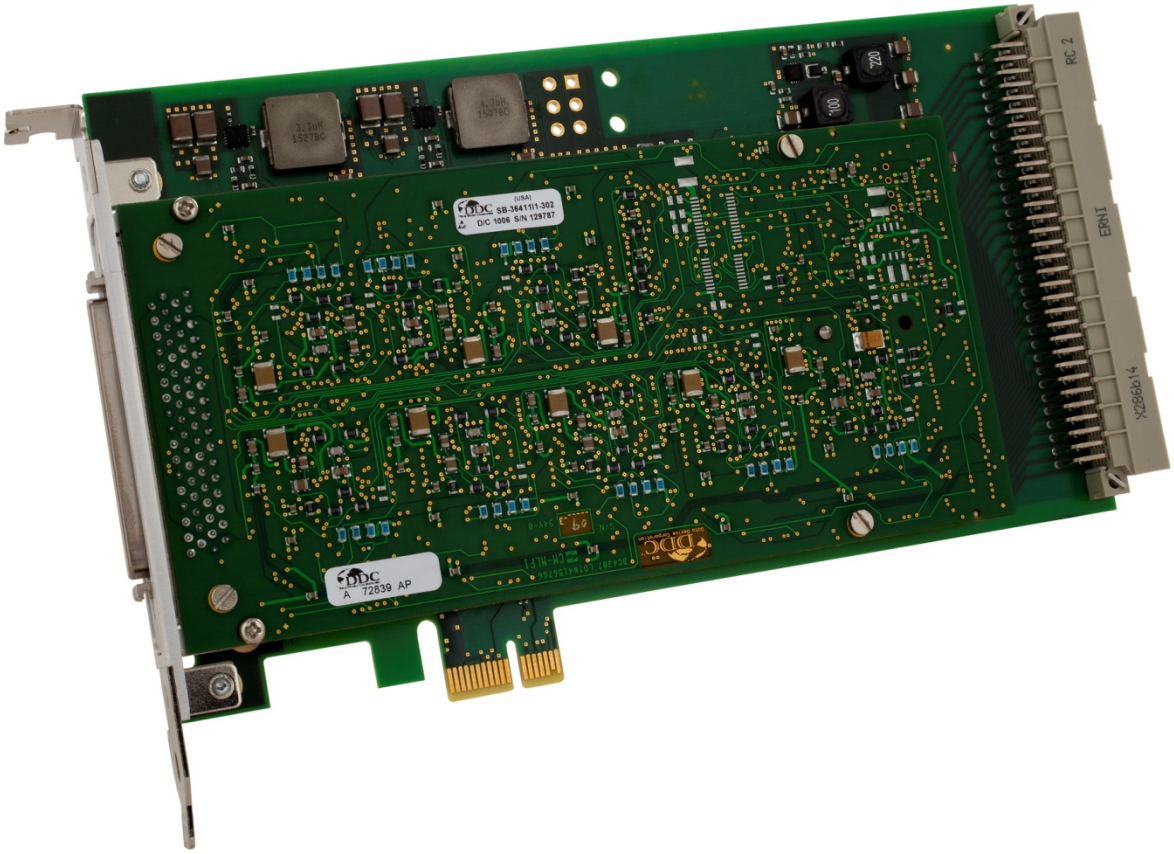


Figure 1. SB-3625XKX Synchro/Resolver-to-Digital PCIe Board

3.3 Applications

The SB-3625XKX is designed for test applications involving angle position measurements from synchro and resolver sensors. Synchros and resolvers are used in applications such as motor control, industrial automation, robotics, antenna positioning, and valve control. This device is ideal for test engineers and developers to perform lab testing on these types of applications. Applications include modern, high performance industrial and military position feedback and control systems. Typical motion feedback applications include motor control, machine tool control, antenna control, robotics and process control systems. The SB-3625XKX is supplied with a Graphical User Interface (GUI) to analyze position information, direction and BIT.

4 SPECIFICATIONS

Table 1. SB-3625XKX Specifications

These specifications apply over the rated power supply, temperature, and reference frequency ranges; 10% signal amplitude variation and 10% harmonic distortion

PARAMETER	UNIT	VALUE			
RESOLUTION	Bits	10, 12, 14, or 16 programmable (note 4)			
ACCURACY		**47 – 1k (note 2)**		**1k – 4k**	**4k – 7k**
Option 0 (2V Single-ended)	Minutes	—		1 + 1 LSB	5 + 1 LSB
Option 1 (11.8V Synchro)	Minutes	—		1 + 1 LSB	5 + 1 LSB
Option 2(11.8V Resolver)	Minutes	—		1 + 1 LSB	5 + 1 LSB
Option 3 (90V Synchro 400Hz)	Minutes	—		2 + 1 LSB	5 + 1 LSB
Option 4 (90V Synchro 60Hz)	Minutes	2 + 1 LSB		—	—
SIGNAL INPUT		**Solid State**			
Option Number		Option 0		Option 1, 2	Option 3, 4
Synchro	Vrms L-L	—		11.8	90
• Zin line-to-line	Ohms	—		52k	195k
• Zin each line-to-ground	Ohms	—		35k	130k
Resolver	Vrms L-L	2 Vrms direct (note 3)		11.8	—
• Zin single ended	Ohms	10M min || 20pf (note 1)		70k	—
• Zin differential	Ohms	N/A		140k	—
Common-mode Range	V max	N/A		30 max	—
REFERENCE INPUT		**Solid State**			
Signal Input Option Number		Option 0	Option 1, 2	Option 3	Option 4
Carrier Frequency	Hz	360 – 7k	360 – 7k	360 – 1k	47 – 400
Type		Differential	Differential	Differential	Differential
Voltage Range	Vrms	2 – 40	2 – 40	50 – 130	50 – 130
Input Impedance					
• single ended	Ohms	100k	100k	300k	300k
• differential	Ohms	50k	50k	200k	200k
Common-mode Range	Vpeak	50	50	200	200
DIGITAL OUTPUTS					
A, B, Zero Index (ZI)		50pf+			
Drive Capability		Logic 0: 1 TTL load, 1.6mA at 0.4V max			
		Logic 1: 10 TTL Loads, = 0.4mA at 2.8V min			
After set into A quad B mode		Logic 0: 100mV max driving CMOS			
		Logic 1: +5V supply minus 100mV min driving CMOS			

Table 1. SB-3625XKX Specifications

These specifications apply over the rated power supply, temperature, and reference frequency ranges; 10% signal amplitude variation and 10% harmonic distortion

PARAMETER	UNIT	VALUE		
POWER SUPPLY		**MIN**	**TYP**	**MAX**
Voltage/Tolerances (per PCIe CEM)				
+3.3V	V	3.003	3.3	3.597
+12V	V	11.04	12	12.96
Current				
+3.3V	A		0.25	
+12V	A		0.25	
COOLING METHOD		Air Cooled		
TEMPERATURE RANGE				
Operating	°C	0 to +55		
Storage	°C	-20 to +75		
PHYSICAL CHARACTERISTICS				
Size	in	7.24 x 4.20 x 0.60		
	(mm)	(183.85 x 106.62 x 15.24)		
Weight	oz	7.41 (max)		
	(g)	(210 (max))		

Table 1 notes:

1. || = “in parallel with”
2. If the frequency in between 47 and 1kHz, then there will be 1 LSB of jitter.
3. Direct input requires SIN input, COS input, and a common ground.
4. Signal input option #4 (90V Synchro 60Hz) not recommended for use in 16 bit resolution mode due to excessive jitter.

5 HARDWARE

5.1 Installation

The ***SB-3625XKX*** board is a PCI Express x1 1.0a compliant board that can be inserted in any standard height PCI Express 1.0a/1.1/2.0 compliant slot. When installing the board, the following should be observed:

- **NEVER** insert or remove the board with the power turned on.
- **ALWAYS** take proper precautions to guard against static damage.
- Use a wrist strap if available, or ensure proper static grounding by touching the power supply cover **WITH POWER OFF**.
- Insert the board and gently press into the PCI Express mating connector. Secure the rear I/O panel bracket with the proper hardware.
- **ALWAYS** secure both rear I/O panel brackets for the ***SB-3625XKX*** option.
- Make sure that adjacent cabling and wiring do not hinder the airflow around the board.

The board is a true Plug and Play device and as such, there are no jumpers or switches to be set for address or interrupt selection. Interrupts and memory selections will be performed by the operating system as the boot system progresses.

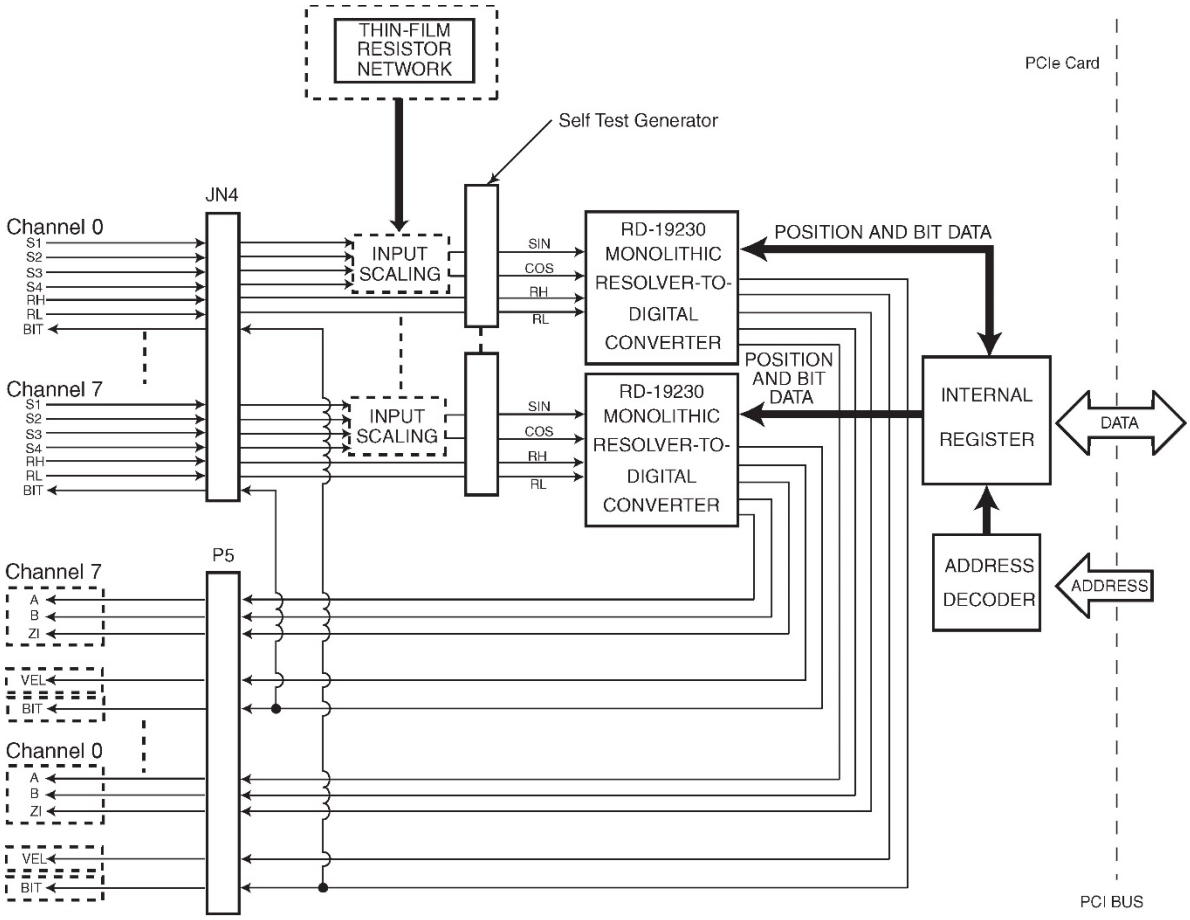


Figure 2. SB-3625XKX PCIe Board Block Diagram

5.2 Configuration

5.2.1 JN4 96-pin Mating Connector

Table 2 lists the pinouts and Figure 3 shows the mechanical assembly for the JN4 mating connector. Row B is No Connect.

Figure 3. JN4 96-Pin Mating Connector

Table 2. JN4 96-Pin Connector Pinout		
Pin Number	**JN4 Row A**	**JN4 Row C**
1	BIT – Channel 1	BIT – Channel 0
2	BIT – Channel 3	BIT – Channel 2
3	BIT – Channel 5	BIT – Channel 4
4	BIT – Channel 7	BIT – Channel 6
5	GND	GND
6	RH – Channel 7	RH – Channel 1
7	RH – Channel 5	RH – Channel 2
8	RH – Channel 6	RH – Channel 3
9	RH – Channel 0	RH – Channel 4
10	GND	GND
11	RL – Channel 1	RL – Channel 5
12	RL – Channel 6	RL – Channel 4
13	RL – Channel 7	RL – Channel 3
14	RL – Channel 0	RL – Channel 2
15	GND	GND
16	S3 (+SIN) – Channel 4	S2 (+COS) – Channel 4
17	S1 (-SIN) – Channel 4	S4 (-COS) – Channel 4
18	S1 (-SIN) – Channel 3	S4 (-COS) – Channel 3
19	S3 (+SIN) – Channel 3	S2 (+COS) – Channel 3
20	GND	GND
21	S3 (+SIN) – Channel 6	S2 (+COS) – Channel 6
22	S1 (-SIN) – Channel 6	S4 (-COS) – Channel 6
23	S3 (+SIN) – Channel 7	S2 (+COS) – Channel 7
24	S1 (-SIN) – Channel 7	S4 (-COS) – Channel 7
25	S3 (+SIN) – Channel 2	S2 (+COS) – Channel 2
26	S1 (-SIN) – Channel 2	S4 (-COS) – Channel 2
27	S3 (+SIN) – Channel 0	S2 (+COS) – Channel 0
28	S1 (-SIN) – Channel 0	S4 (-COS) – Channel 0
29	S1 (-SIN) – Channel 1	S4(-COS) – Channel 1
30	S3 (+SIN) – Channel 1	S2 (+COS) – Channel 1
31	S1 (-SIN) – Channel 5	S4 (-COS) – Channel 5
32	S3 (+SIN) – Channel 5	S2 (+COS) – Channel 5

Note: Each channel should have its own return / gnd allocated in the cabling. There should not be one common ground for all channels.

5.2.2 P5 68-Pin Connector

Table 3 lists the pinout and Figure 4 shows the mechanical assembly for the mating connector.

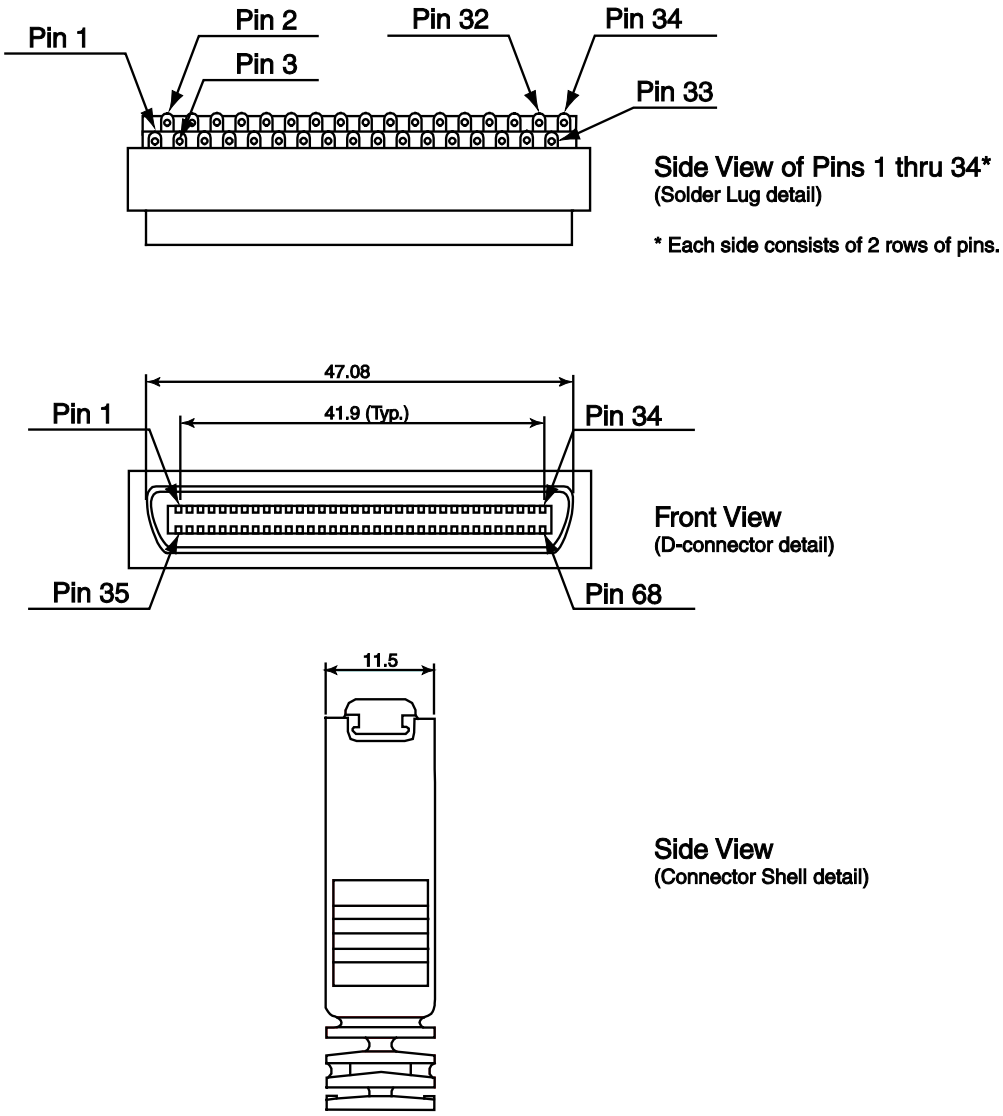


Figure 4. P5 68-Pin D-Type Mating Connector

Suggested Mating Connector:

- 68-pin connector solder plug and junction shell : Acon HBW-3268K-3207
- Ribbon : 3M-10168-6000EC
- Board has 3M 68-pin connector N10268-5242 VC

Table 3. P5 68-Pin Connector Pin Out			
PIN	**NAME**	**PIN**	**NAME**
1	Velocity_Channel 0	35	A_Channel 4
2	Velocity_Channel 1	36	A_Channel 5
3	GND0	37	B_Channel 4
4	GND1	38	B_Channel 5
5	Velocity_Channel 2	39	ZI_Channel 4
6	Velocity_Channel 3	40	ZI_Channel 5
7	GND2	41	GND12
8	GND3	42	GND13
9	Velocity_Channel 4	43	A_Channel 6
10	Velocity_Channel 5	44	A_Channel 7
11	GND4	45	B_Channel 6
12	GND5	46	B_Channel 7
13	Velocity_Channel 6	47	ZI_Channel 6
14	Velocity_Channel 7	48	ZI_Channel 7
15	GND6	49	GND14
16	GND7	50	GND15
17	Spare0	51	Spare2
18	Spare1	52	Spare3
19	A_Channel 0	53	BIT_Channel 0
20	A_Channel 1	54	BIT_Channel 1
21	B_Channel 0	55	BIT_Channel 2
22	B_Channel 1	56	BIT_Channel 3
23	ZI_Channel 0	57	GND16
24	ZI_Channel 1	58	GND17
25	GND8	59	BIT_Channel 4
26	GND9	60	BIT_Channel 5
27	A_Channel 2	61	BIT_Channel 6
28	A_Channel 3	62	BIT_Channel 7
29	B_Channel 2	63	Spare4
30	B_Channel 3	64	Spare5
31	ZI_Channel 2	65	Spare6
32	ZI_Channel 3	66	Spare7
33	GND10	67	Spare8
34	GND11	68	Spare9

6 DETAILED ARCHITECTURE

6.1 Mechanical Outline

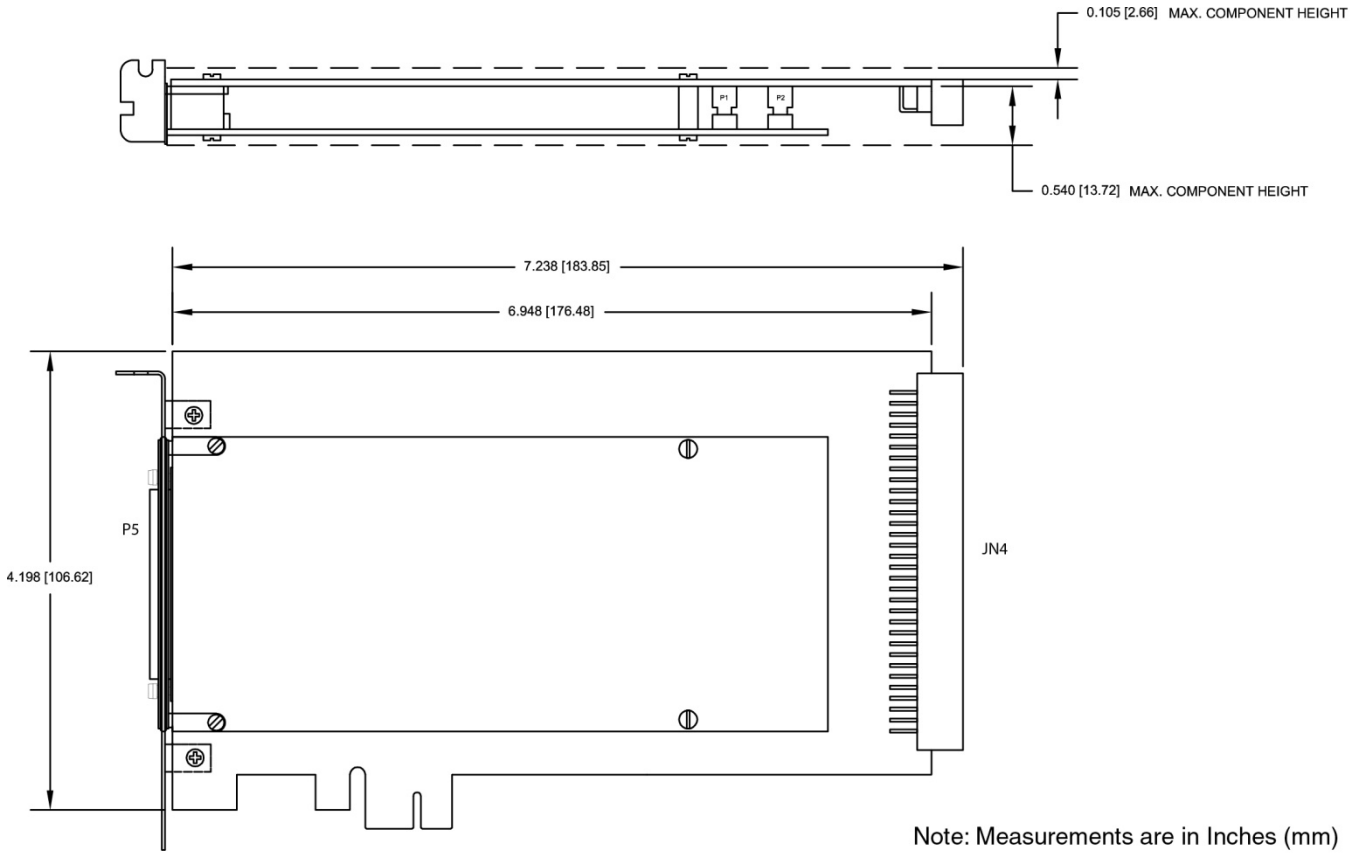


Figure 5. SB3625XKX Mechanical Outline

6.2 Synchro / Resolver to Digital Channels

6.2.1 Signal Connections

- Synchro Mode Connect S1, S2, S3
  - S1 = X
  - S2 = Z
  - S3 = Y
- Resolver Mode Connect
  - S3 = +SIN
  - S1 = -SIN
  - S2 = +COS
  - S4 = -COS
- Single ended mode connections.
  - When using 2V single ended configurations, S1 and S4 on board connector are no-connect. Use associated analog ground per output channel for S1 and S4 resolver outputs used.

6.2.2 Bandwidth

The user can program the device through software for each input channel independently for Low bandwidth (15/45 Hz) or High bandwidth (100/300 Hz) depending on order selection. Refer to Table 4 for dynamic characteristics.

Use caution when operating in 10-bit and 12-bit modes. Large input steps can induce a high acceleration into the R/D converter that may cause the maximum velocity to be exceeded. If this occurs, the converter can enter a spin-around condition where it may never settle to an angle because of the low bandwidths at these resolutions.

Table 4. Dynamic Characteristics

TYPE		60 Hz NOMINAL				400 Hz NOMINAL			
RESOLUTION (bits)		10	12	14	16	10	12	14	16
BANDWIDTH (Hz)	Low	*	*	15		*	*	100	
	High	45		**	**	300		**	**
TRACKING RATE (rps)		32	8	2	.5	320	80	20	5
SCALE FACTOR (Volts/rps)		.125	.5	2	8	.0125	.05	.2	.8

*Not recommended - Low bandwidths in low resolutions may induce spin around and the part will not settle
**High bandwidths in high resolutions may be used with carrier frequencies above 1.5 kHz

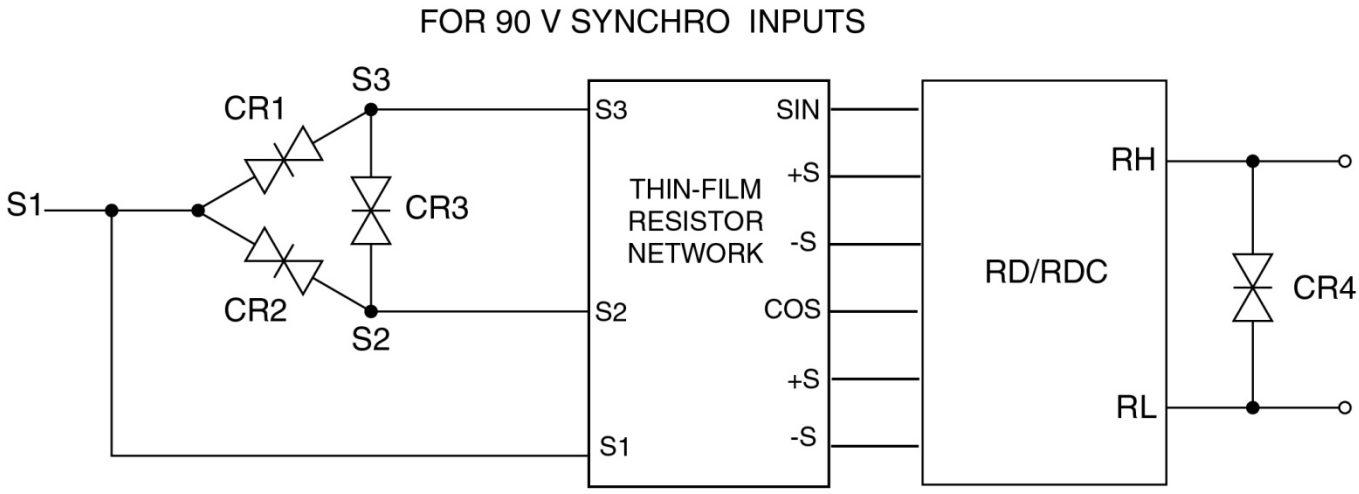
6.2.3 Synthesized Reference

The synthesized reference eliminates errors due to phase shift within the synchro/resolver sensor of up to 45° between the reference and the signal inputs. This feature is built into all input channels of this device.

6.2.4 Transient Protection

Systems using the 90 V line-to-line inputs may have voltage transients which exceed the maximum specification for the thin-film resistor network (500 V). The 90 V may be derived from poorly regulated 115 V Power Supplies, which have various high current loads. These loads switch on and off, thus causing spikes and transients in regulation. These transients can destroy the input thin-film resistor network. Therefore, 90 V line-to-line solid state input (DDC-49590) thin-film may be protected by installing voltage suppressors as shown in Figure 6 and Figure 7.

Voltage transients are also likely to occur whenever the synchro or resolver input is switched on and off. For instance, a 1000 V transient can be generated when the primary of a control transmitter (CX) or torque transmitter (TX) driving a synchro or resolver input is opened.



CR1, CR2, CR3, and CR4 are 1.5KE170CA or 1.5KE200C-type bipolar transient voltage suppressors or equivalent.

Figure 6. Voltage Transient Suppressor, 90V Synchro Input

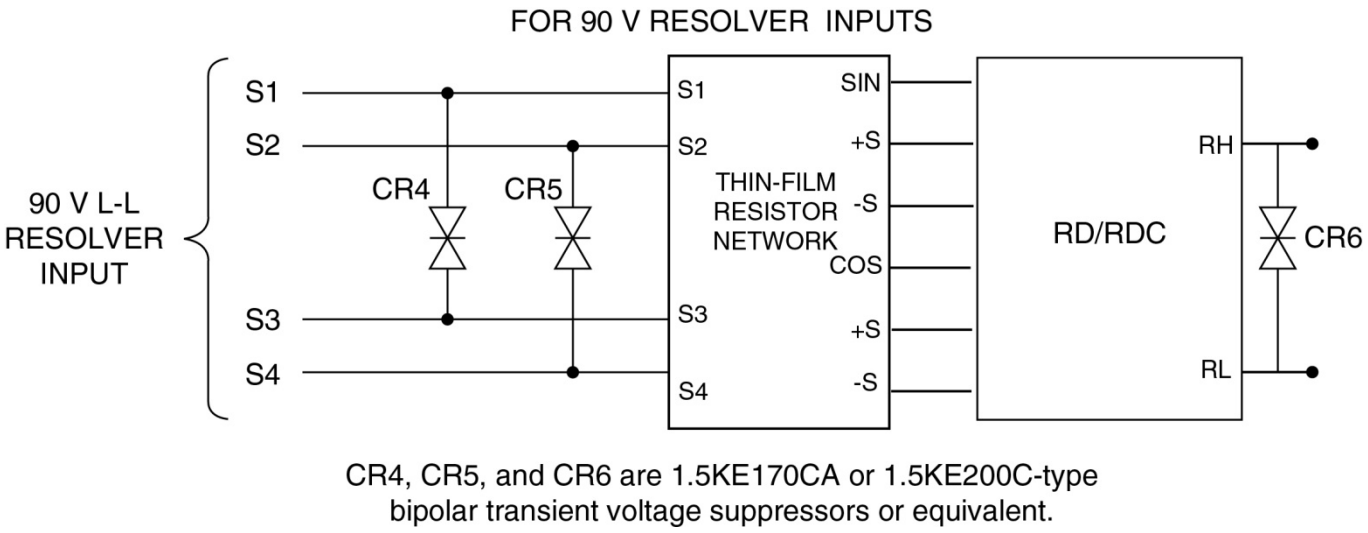


Figure 7. Voltage Transient Suppressor, 90V Resolver Input

6.2.5 Incremental Encoder Emulation (A Quad B)

The device can also be used for incremental encoder emulation. The following outputs are readily available A, B, and ZIP (Zero Index Pulse). The timing of the A, B output is dependent on the rate of change of the synchro/resolver position (rps or degrees per second) and the encoder resolution latched into the converter (refer to Figure 6). The calculations for the timing are:

n = resolution of parallel data

t = 1 / (2n * Velocity(RPS))

T = 1 / (Velocity(RPS))

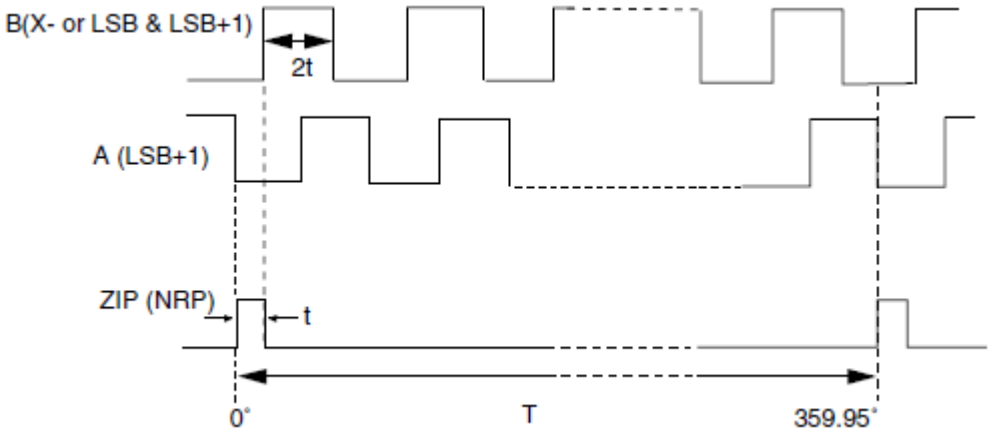


Figure 8. Incremental Encoder Emulation Timing

6.2.6 Velocity Output

Each input channel has an analog velocity output . The analog velocity output is accessible through connector P5. The voltage range is +/- 4V. The polarity indicates the direction of rotation where a positive voltage is for increasing angle. See Table 5 below for analog velocity characteristics.

Table 5. Velocity Characteristics

PARAMETER	UNITS	TYPICAL	MAX./MIN.
POLARITY			
Voltage Range	V	4.0	
VOLTAGE SCALING			
(resolution dependent)	RPS/V	Typical TR (See Table 4)	
SCALE FACTOR			
Error	%	10	20 (max.)
Scale Factor TC	PPM/ deg C	100	200 (max.)
Reversal Error	%	1	2 (max.)
Linearity	% output	0.5	1 (max.)
Zero Offset	mV	5	15 (max.)
Zero Offset TC	uV/ deg C	15	30 (max.)
Load	k Ohms		10 (min.)

6.2.7 Built-in-Test (BIT) Output

The Built-In-Test (BIT) will flag Loss-of-Signal (LOS), Loss-of-Reference (LOR), Loss-of-Tracking (LOT), and 180° phase error fault conditions. The BIT output is active low and a logical OR of these four conditions. Any one or combination of these conditions will assert the BIT output. These fault conditions are described in Table 6 below. Also, excessive error is detected when the difference between the analog input and the digital output exceeds approximately 100 LSBs of positive or 250 LSBs of negative error (in the selected resolution), the BIT will be asserted.

Table 6. BIT Fault Conditions

Fault Condition	Descritption
LOS	Both SIN and COS inputs (S1-S3, S2-S4) must fall below 0.5 Vrms.
LOR	The reference input (RH-RL) must fall below 0.5 Vrms.
LOT	This condition occurs when the difference between the anlog input and digital output exceeds 100 lsbs in the positive direction or 250 lsbs in the negative direction. This typically occurs when exceeding the maximum tracking rate or during power up.
180° Phase Error	180° phase error input signal to reference input (false null) causes a BIT plus kickstarts the converter counter to correct the error.

6.2.8 Two Speed

Two speed allows resolutions greater than 16 bits to be achieved. Refer to the RD/RDC Applications manual (MN-19220XX-001) and the Synchro/Resolver Conversion Handbook. These documents are available at www.ddc-web.com.

6.2.9 Self-Test

The device has a built-in self-test capability which can run a simulated test angle of 0, 45, or 90 degrees on each channel. Any channel not reporting back an answer within ± 1° will fail.

7 SOFTWARE

Numerous software packages are available for the SB-3625. The DDC software packages are developed to allow shorter design cycles while allowing all SB-3625 functionality to be accessed by user level code. Note that the SB-3625 will appear as SB-3641 within the computer system, which is the respective base PMC board.

The available software packages include:

- Motion Feedback C SDK (SB-36030Sx)
- Motion Feedback Application (SB-36000S0)
- Motion Feedback LabVIEW SDK (SB-36030SL)

7.1 Software Overview

7.1.1 Motion Feedback C SDK (SB-36030Sx)

The card is supplied with the SB-36030Sx Motion Feedback C SDK. This software development kit includes a runtime library that provides the user with a hardware abstraction layer for the DDC Motion Feedback hardware. This software layer includes the routines that dramatically reduce software development time by providing high-level C functions for the application programmer to interface to the card. C samples are included with the library to demonstrate how the API works with the hardware. Table 7 shows a summary of the supported operating systems.

The ***SB-36030Sx Software Manual*** can be downloaded from the DDC web site at *www.ddc-web.com*.

Table 7. Motion Feedback Library C SDK Part Number Descriptions

Part Number	Operating System
SB-36030S0	Windows
SB-36030S1	Linux

7.1.2 Motion Feedback Application (SB-36000S0)

The card is supplied with the SB-36000S0 Motion Feedback Application. This is a graphical software which runs on Windows.

The ***SB-36000S0 Manual*** can be downloaded from the DDC web site at www.ddc-web.com.

7.1.3 Motion Feedback LabVIEW SDK (SB-36030SL)

The card is supplied with the SB-36030SL Motion Feedback LabVIEW support package. This software development kit includes a set of VIs that provides the user with a hardware abstraction layer for the DDC Motion Feedback hardware in a LabVIEW environment. The Package includes 3 layers of VIs which enable easy application development. Functional user samples are included for common functions.

7.1.4 Troubleshooting the Installation

Usually the installation will be successful, and the self-test within the sample programs will pass. There are, however, some situations that can cause problems during the installation. The most common are detailed below.

An error is returned when an attempt is made to run any of the samples. This fault is almost always related to an incorrectly assigned device number. Be sure that a device number was correctly assigned through the DDC Card Manager.

If an error is encountered and the device number appears to be correctly assigned, check the operating system. The BIOS setting for a PnP operating system is sometimes set to YES, which can cause a problem. This BIOS option must be set for NO. The operating system, as well as all hardware on your system, will still maintain PnP compatibility; it will not be necessary to manually configure resources for PnP cards.

8 ORDERING INFORMATION

SB-3625X K X – JL 1

Accuracy:
1 = 1 minute accuracy

Environmental Temperature Options:
JL = 0°C to +55°C Operating Temperature Range, Lab non-rugged

Number of Channels:
8 = 8 Channels
4 = 4 Channels

Signal Input Options:

#	Type	Programmable Bandwidth Range (note 3)
0	2V Single Ended	100/300Hz
1	11.8V Synchro	100/300Hz
2	11.8V Resolver	100/300Hz
3	90V Synchro	100/300Hz
4	90V Synchro (60Hz) (note 1)	15/45Hz

Notes:
1. 90V Synchro 60Hz not recommended for use in 16-bit resolution mode.
2. The above products contain tin-lean solder.
3. Bandwidth range selections are user programmable independently for each channel. Bandwidth range is dependent on the Signal Input option in the ordering information above.

INCLUDED ACCESSORIES

- 2 mating connectors

STANDARD DDC PROCESSING FOR DISCRETE MODULES/PC BOARD ASSEMLIES		
TEST	**METHOD(S)**	**CONDITION(S)**
INSPECTION/WORKMANSHIP	IPC-A-610	Class 3
ELECTRICAL TEST	DDC ATP	—